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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/770,890	02/02/2004	James M. Derderian	2269-4817.3US (01-0103.03)	1094
24247	7590	04/11/2007	EXAMINER	
TRASK BRITT P.O. BOX 2550 SALT LAKE CITY, UT 84110			THAI, LUAN C	
			ART UNIT	PAPER NUMBER
			2891	
SHORTENED STATUTORY PERIOD OF RESPONSE		MAIL DATE	DELIVERY MODE	
3 MONTHS		04/11/2007	PAPER	

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)
	10/770,890	DERDERIAN, JAMES M.
	Examiner Luan Thai	Art Unit 2891

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 01 February 2007.
 2a) This action is **FINAL**. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-33 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 1-33 is/are rejected.
 7) Claim(s) _____ is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on 02 February 2004 is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) <input type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
	6) <input type="checkbox"/> Other: _____

DETAILED ACTION

Request for Continued Examination

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 2/1/07 has been entered.

Claims 1-33 are pending in this application.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-5, 7-25 and 31-33 are rejected under 35 U.S.C. 102(e) as being anticipated by LoBianco et al. (6,340,846 of record).

Regarding claims 1, 11, 16, 24, LoBianco et al. teach (see specifically figures 3-7, Col. 3, line 30 to Col. 6, line 45) a method for forming an assembly including

semiconductor devices in stacked arrangement, comprising: providing a substrate (12) including a plurality of contact areas (26), mounting a first semiconductor device (14) on the substrate (12) via an adhesive (13), establishing electrical communication between the substrate (12) and the first semiconductor device (14) by using discrete conductive elements (e.g., conductive wires 38) to electrically connect the contact areas (26) of the substrate and the bond pads (34) on the active surface of the first semiconductor device (14), applying substantially a predetermined volume of adhesive material (40) to an active surface of a first semiconductor device (14) (Col. 3, lines 62+ and Col. 4, lines 1-11), positioning a second semiconductor device (16) adjacent to the first semiconductor device (14), the adhesive material (40) securing the second semiconductor device (16) to the first semiconductor device (14) and spacing a bottom surface of the second semiconductor device (16) a predetermined distance apart from the active surface of the first semiconductor device (Col. 4, lines 28+). Since a desired thickness of the adhesive layer (42) disposed between the first and second devices (14/16) is obtained (Col. 4, lines 28-30), such thickness or the distance between the active surface of the first device (14) and the bottom surface of the second device (16) must be a permanent distance.

Regarding claims 2-4, LoBianco et al. further teach the adhesive material (40) being applied over the discrete conductive elements (38) (Fig. 5, Col. 4, lines 53+), and the second semiconductor device (16) being positioned partially over or on the discrete conductive elements (38).

Regarding claim 5, since the adhesive material (40) is applied to the active surface of the first semiconductor device (12) and the second semiconductor device (14) is

positioned adjacent to the first semiconductor device via the adhesive material (40), such adhesive material (40) is considered as being introduced between the first and second semiconductor devices.

Regarding claim 7, LoBianco et al. further disclose the adhesive material (40) substantially encapsulating portions of the discrete conductive elements (38) (Col. 4, lines 53+).

Regarding claims 8-9, 13-14 and 31-32, although LoBianco et al. do not clearly teach the adhesive (40) being substantially cured to at least “*a semisolid state*”, this feature is taken to be inherent in LoBianco et al. method since the fluid adhesive (40) (Col. 3, liens 63+) being cured to solidify it is disclosed (Col. 5, lines 10+), and it is apparent that “a semisolid state” must exist when the adhesive (40) is changed from “a fluid state” to “a solid state” through the curing or hardening process.

Regarding claims 10, 12, 15, 25 and 33, LoBianco et al. do disclose that the adhesive (40), which is applied between the two opposing surfaces of the first and second semiconductor devices (12/14), is a Hysol-4451 (Col. 3, liens 63+), and the cured Hysol-4451 appears to be shrinkage between 5-10% as evidenced by Belke (US Pat. No. 6,326,241, Col. 6, lines 37+ and lines 45+). Since the active surface of the first semiconductor device (14) is spaced apart from the bottom surface of the second semiconductor device (16) by the fluid adhesive (40) of Hysol-4451, which appears to be shrinkage through the curing or hardening step, the distance between the active surface of the first semiconductor device (14) and the bottom surface of the second semiconductor device (16) is inherently reduced a distance when the fluid adhesive (40) of Hysol-4451

is cured or hardened to change from a fluid state to a solid state. In other words, the second semiconductor device (16) must be drawn toward at least the first semiconductor device (14) while the adhesive (40) of Hysol-4451 is shrinking through the curing or hardening step.

Regarding claims 17-19, LoBianco et al. also disclose that applying substantially a predetermined volume of adhesive material (40) to an active surface of a first semiconductor device (14), as described above, is effected following establishing electrical communication between the substrate (12) and the first semiconductor device (14); positioning the second semiconductor device (16) adjacent to the first semiconductor device (14) follows applying substantially a predetermined volume of adhesive material (40) to an active surface of a first semiconductor device (14); and applying substantially a predetermined volume of adhesive material (40) to an active surface of a first semiconductor device (14) follows positioning the second semiconductor device (16) adjacent to the first semiconductor device (14) (Col. 3, line 55 to Col. 6, line 45).

Regarding claims 20-21, LoBianco et al. further disclose that the end portion of the discrete conductive element (38) that is bonded to the bond pad (34) of the first semiconductor device (14) is protruded above the surface of the first semiconductor device (14), and the second semiconductor device (16) is positioned over the first semiconductor device (14) and at least partially over at least one discrete conductive element (38) protruding above the active surface of the first semiconductor device (14) (see Fig. 3).

Regarding claim 22, LoBianco et al. further disclose the conductive elements (38) comprising wire bonding bond pad to corresponding contact areas (26) (Col. 3, lines 56+).

Regarding claim 23, LoBianco et al. also teach encapsulating at least portions of the first semiconductor device (14), the second semiconductor device (16), the discrete conductive elements (38), and the substrate (12) by encapsulant (60) (Fig. 6, Col. 5, lines 25+).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 6 and 26-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over LoBianco et al. (6,340,846 of record) in view of Heo (6,555,917 of record).

Regarding claims 26-28 and 30, LoBianco et al. disclose the claimed invention including the method steps of applying substantially the predetermined volume of adhesive material (40) onto the active surface of the first semiconductor device (14) and positioning the second semiconductor device (16) adjacent to the first semiconductor device via adhesive (40) as described above. LoBianco et al., however, fail to teach the step of applying (or introducing) adhesive step being performed following the step of positioning of second semiconductor device.

Heo while related to a similar method of making a stacked semiconductor devices teaches (see specifically figures 1 and 4, Col. 2, line 55 to Col. 5, line 40) a first semiconductor chip (10-1) mounted on the substrate (12) via an adhesive (28), wire bonding the bond pads (16) formed on the active surface of the first semiconductor device (10-1) to the contact areas (18) on the substrate (12), applying or introducing an amount of adhesive material (36) onto the active surface of the first semiconductor device (10-1) and positioning the second semiconductor device (10-2) adjacent to the first device via adhesive (36), wherein the step of applying or introducing adhesive material can be performed before positioning the second semiconductor device on the first semiconductor device or *the adhesive material can be injected with a syringe to fill the gap between the first semiconductor device and second semiconductor device after or following the step of positioning the second semiconductor device on the first device* (Col. 4, line 66 to Col. 5, lines 8). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the LoBianco et al.'s method of stacking the second device on the first device by performing the step of positioning second semiconductor device adjacent to the first semiconductor device before applying or injecting an amount of adhesive material with a syringe to fill the gap between the first and second semiconductor devices, since such method step is commonly applied in the art as being taught by Heo, and such modification is held to be within the ordinary designing ability expected of a person skilled in the art.

Regarding claims 6 and 29, the proposed method of LoBianco et al. and Heo teaches the claimed invention including introducing or injecting adhesive material into

the gap or space between the first and second semiconductor devices as detailed above except for teaching that injecting adhesive material would force the surface of the second semiconductor device away from at least the first semiconductor device. This claimed feature is considered to be obvious since one skilled in the art would understand that injecting adhesive material into the gap or space between the first and second semiconductor devices, as disclosed by LoBianco et al., would obviously force the surface of the second semiconductor device away from at least the first semiconductor device.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Luan Thai whose telephone number is 571-272-1935. The examiner can normally be reached on 8:00 AM - 4:30 PM, Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bradley W. Baumeister can be reached on 571-272-1722. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Luan Thai
Primary Examiner
Art Unit 2891
March 31, 2007